Applicants respectfully traverse the rejections. However, for purposes of compact prosecution, Applicants have amended the claims to further clarify Applicants' invention.

For example, claim 1 now recites, *inter alia*:

A media processing system, comprising:

... digital data including video data that is compressed in a first standardized format;

... means for decoding said first standardized format compressed video images to generate full motion video pixel data;

... wherein the means for decoding the first standardized format compressed video images is adapted for reconfiguration to decode digital data including data that is compressed in a second standardized format.

Claim 12 now contains a similar limitation. Claim 21 is a method claim that now contains an analogous limitation.

Support for the amendments to claims 1, 12 and 21 can be found at page 13, lines 9-12 where Applicant's state that "the MPEs may adapt to the newest standards and algorithms since the instructions easily can be changed to carry out the new algorithms."

Neither Cloutier nor any of the other cited references teach or suggest means for decoding compressed video data according to a first standardized format that can be reconfigured to decode compressed video data according to a second standardized format. Accordingly, claims 1, 12 and 21 are patentable over the cited references.

Claims 2-11, 13-20, 22 and 23 all depend from claims 1, 12 or 21, and thus, are allowable as being directed to specific novel substitutes as well as by depending from allowable parent claims.

New Claims 24 and 25

New claims 24 and 25 have been added to claim additional novel aspects of the present invention. Applicants respectfully submit that new claims 24 and 25 are allowable over the prior art. In addition, Applicants submit that no new matter has been added by the addition of the new claims.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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On page 11 of the specification, replace the paragraph beginning at line 5 with:

After all the audio, video and DVD information is decoded and placed in memory, display generator 80 retrieves the video, subpicture and control information from memory and performs some processing. For example, in accordance with one embodiment of the present invention, the video information is stored in memory in 4:2:0 MPEG format. Display generator 80 [preferably]converts the 4:2:0 format to 4:2:2 format, which is consistent with CCIR 656 standard video format. In addition, display generator 80 [preferably]combines video information with overlay information, such as menus and the like, and subpicture channel information and presents the entire packet of information as an output. Finally, display generator 80 [preferably]is configured to perform video timing and refresh functions, and may perform some of the subpicture decoding operations. A more detailed description of how display generator 80 interacts with one or more of the MPEs to perform subpicture decode is set forth in U.S. Patent Application No. 09/476,698[_____ (Attorney Docket No. 19223-000700US)], filed January 3, 2000[_____], and entitled "Subpicture Decoding Methods and Apparatus," the entirety of which is incorporated herein by reference.

On page 14 of the specification, replace the paragraph beginning a line 4 with:

Architecture 100 of the MPEs may have a plurality of sub-units, such as an execution control unit (ECU) 106, a memory processing unit (MEM) 108, a register control unit (RCU) 110, an arithmetic logic unit (ALU) 112, a multiplication processing unit (MUL) 114, and a register file 116. In one embodiment[Preferably], ECM 106, MEM 108, RCU 110, ALU 112 and MUL 114 all are connected together in parallel via register file 116. An Instruction Decompression and Routing unit 118 is connected to an instruction memory 120 via instruction bus 102, and [preferably]is configured to decode[s] and route[s] instructions to the various processing units within the MPE.

Instruction memory 120 stores a plurality of instructions, which control the various processing units in the MPE. The stored instructions are in the form of very long instruction word (VLIW) instructions, which, in one embodiment, [preferably]have been compressed to reduce the amount of memory required to store the instructions. A more detailed discussion of the VLIW compression is set forth below.

On pages 22 and 23 of the specification, replace the paragraph beginning at line 29 of page 22 with:

ALU 112 [preferably]includes a plurality of switches 210, 212, and 214, such as multiplexers or the like, which are configured to select data from one of a number of source inputs of ALU 112. For example, switch 210 may select data from a Src A, which in accordance with the present invention is a 32-bit data type stored in any one of the registers, or from immediate data (ImmB) stored in the ALU instructions. Similarly, second switch 212 may select data from Src A, or from an immediate value (ImmA) stored in the ALU instruction. The ImmA immediate data also [data]may be sign extended by a sign extender 216 prior to entering the switch. The ImmA data, Src B data, Src D data, or the most significant bits of Src B data may be selected by third switch 214. The most significant bits of Src B data may be determined by a most significant bit (MSB) unit 217.

IN THE CLAIMS:

1. (Amended) A media processing system, comprising:

DRAM having a plurality of storage locations for storing digital data being processed by said media processing system, said digital data including video data that is compressed in a first standardized format;

means for processing said digital data that includes said first standardized format compressed video data to produce compressed video images and image data;

means for decoding said first standardized format compressed video images to generate full motion video pixel data;

means for sharing said DRAM between said processing means and said decoding means; and

means for producing a full motion video signal from said full motion video pixel data;

wherein the means for decoding the first standardized format compressed video images is adapted for reconfiguration to decode digital data including data that is compressed in a second standardized format.

2. (Amended) The system as recited in claim 1, wherein said compressed video data comprises a plurality of pixels, and said first standardized compressed format comprises a luminance sample generated for each pixel, and two chrominance samples generated for every four pixels.

10. (Amended) The system as recited in claim 1, wherein said DRAM stores audio data that is compressed in a standardized format, and further comprising means for decompressing said audio data that is compressed in a first standardized format to generate uncompressed audio data, and means for combining said full-motion video data and said uncompressed audio data to generate full-motion multimedia data.

12. (Amended) A single semiconductor chip media processor, comprising:

a semiconductor memory, internal to said single semiconductor chip, for storing digital data, including video digital data compressed in first standardized format;

means for processing said compressed video data in said semiconductor memory to produce color, full motion video data that is temporarily stored in said semiconductor memory;

means for decoding said color, full motion video data stored in said semiconductor memory to generate color, full motion video image data; and

means for producing a color, full motion video image signal;

wherein the means for decoding said color, full motion video data is adapted for reconfiguration to decode video data compressed in a second standardized format.

13. (Amended) The processor as recited in claim 12, wherein said first compressed video data comprises a plurality of pixels, and said processing means comprises means for multiplying a first pixel with a second pixel in a single clock cycle of said processing means.

19. (Amended) The processor as recited in claim 12, wherein said DRAM stores audio data that is compressed in a first standardized format, and further comprising means for decompressing said audio data that is compressed in[a] the first standardized format to generate uncompressed audio data, and means for combining said full-motion video data and said uncompressed audio data to generate full-motion multimedia data.

21. (Amended) A method of processing media, comprising:

storing digital data being processed by said media processing system in a DRAM, said digital data including video data that is compressed in a first standardized format;

processing said digital data that includes said first standardized format compressed video data to produce compressed video images and image data;

decoding said first standardized format compressed video images to generate full motion video pixel data;